Domynik ARINC 664 End System IP

2-port hardware End System IP core with full ARINC 664 Part 7

VL management, BAG scheduling, UDP / IP / ICMP / ARP filtering

Up to 512 VL table entries — PCIe Gen 2 or AXI4 64-bit host interface

Encrypted RTL, ITAR free — avionics networks. 3 proven FPGA targets.

- **2** Ethernet Ports
- **1 Gbps** Max Ethernet Link Speed
- **50 µs** Frame Latency - 1522 Bytes
- **ARINC 664p7** Compliant
- **DO-254** DAL-A package available

KEY FEATURES

- 2-port End System — ARINC 664 Part 7
- 512 VL table entries
- Protocols: ARINC 664p7, IP, UDP, TCP, ICMP, ARP
- 2-level QoS traffic prioritization
- Host interface: PCIe Gen 2 or AXI4 64-bit slave
- UDP offloading — hardware VL scheduling
- Hardware-only data path — no software latency
- Configurable BAG: 1, 2, 4, 8, 16, 32, 64, 128 ms

SUPPORTED STANDARDS

- ARINC 664 Part 7 — End System
- IEEE 802.3 — Ethernet (GMII, MII)
- RFC 791 — IP Layer 3
- RFC 768 / 793 — UDP / TCP
- RFC 826 — ARP / RFC 792 — ICMP

TRAFFIC MANAGEMENT

- Per-VL Bandwidth Allocation Gap (BAG) enforcement
- UDP filtering and routing per Virtual Link
- 2-level QoS priority classes — hardware data path

DESIGN ASSURANCE

- DO-254 DAL-A — package available (AXI4 variant)
- AMC 20-152A — COTS IP objectives IP-1 to IP-7
- AMC 20-189 — Open Problem Reports

INTERFACES

Ethernet Media	GMII (1 Gbps), MII (100 Mbp
Ethernet Ports	2 ports
Max Link Speed	1 Gbps per port
Host Interface	PCIe Gen 2 or AXI4 64-bit
External Memory	None required

PERFORMANCE

Core Frequency	200 MHz
Frame Latency	50 µs (1522-byte frame)
VL Table	512 entries
QoS Levels	2 priority classes

SOFTWARE

Configuration Tools

Two tools are included to configure and deploy the IP. Both run on Linux.

- Konfyguratr — reads user parameters and generates the IP configuration file
- Loadr — loads the configuration file into the IP at runtime

Host Driver

A host driver is delivered in full C source code, depending on the variant:

- VxWorks — PikeOS

Other OS (Linux, Windows) available on request — contact CetraC.

DELIVERY PACKAGE

Core IP
IEEE 1735-2014 encrypted RTL — technology-independent

Reference Design
Example implementation per variant — see variants table

Konfyguratr
IP configuration file generator — runs on Linux

Loadr
Configuration file loader into the IP — runs on Linux

Host Driver
Full C source code — VxWorks or PikeOS (other OS on request)

Documentation
Functional specification & integration guide

DO-254 DAL-A Package (option)
Available for the Stratix 10 (AXI4) variant — on request for PCIe variants

REFERENCE DESIGN

Reference designs are available on three FPGA families, with project files and timing constraints. See the variants table below.

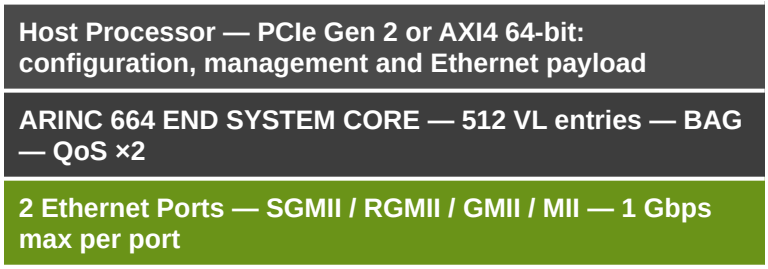
Other FPGA families and ASIC process nodes are supported — contact support@cetrac.io.

FPGA families	Kintex-7, Arria 10, Stratix 10
Board references	Domynik board — others: contact CetraC
Ethernet PHY	SGMII or RGMII
Host interface	PCIe Gen 2 or AXI4
Core frequency	200 MHz
VL table	512 entries
Synthesis tools	Vivado, Quartus

ARCHITECTURE OVERVIEW

Domynik is a fully hardware-implemented End System compliant with ARINC 664 Part 7. All VL management, BAG enforcement and UDP/IP/ICMP/ARP filtering run in the data path at line rate with no software involvement. The host interface (PCIe Gen 2 or AXI4 64-bit slave, depending on the variant) gives the host processor access to Ethernet payload and configuration registers.

The Domynik IP core is delivered as IEEE 1735-2014 encrypted RTL and is not tied to any specific FPGA family or ASIC process node. Synthesis, place-and-route and timing closure are performed by the integrator on their target. Reference designs on Xilinx Kintex-7, Altera Arria 10 and Altera Stratix 10 are provided as integration examples.



Physical interfaces depend on target platform — see Reference Design

AVAILABLE VARIANTS & REFERENCE DESIGNS

	Kintex-7	Arria 10	Stratix 10
Host interface	PCIe Gen 2	PCIe Gen 2 (x8)	AXI4 64-bit slave
FPGA part number	Xilinx Kintex-7 (XC7K160T-2FFG676I)	Altera Arria 10 (10AS066H2F34I1SG)	Altera Stratix 10 (1SX280HU2F50E1VGAS)
Ethernet PHY (ref. design)	SGMII — 2 ports	RGMII — 2 ports	Contact CetraC
Board reference	Contact CetraC	Domynik board	Contact CetraC
Host driver (C source)	VxWorks	PikeOS	On request
LUT / BRAM	Contact CetraC	102k / 11.8 Mbits	Contact CetraC
Synthesis tool	Vivado	Quartus 17.0 Standard	Quartus
Bitstream included	Contact CetraC	Yes	Contact CetraC
DO-254 DAL-A package	Option	Option	Available

Detailed top-level diagram for each variant available in the technical datasheet.