Domynik TSN End System IP

2-port hardware Time-Sensitive Networking (TSN) End System IP core
IEEE 802.1AS sync, 802.1Qbv scheduling, UDP / IP / ICMP / ARP filtering
8-level QoS, PCIe Gen 2 host interface, discrete I/O
Encrypted RTL, ITAR free — deterministic in-vehicle networks (NGVA).

- **2** Ethernet Ports
- **1 Gbps** Max Ethernet Link Speed
- **50 µs** Frame Latency - 1522 Bytes
- **TSN** 802.1AS / 802.1Qbv
- **PCIe** Gen 2 Host Interface

KEY FEATURES

- 2-port TSN End System
- Protocols: IP, UDP, TCP, ICMP, ARP
- 8-level QoS traffic prioritization
- 1× PCIe Gen 2 host interface
- IEEE 802.1AS gPTP sync — no BMCA
- IEEE 802.1Qbv time-aware scheduling
- Discrete I/O interface — hardware-only data path

SUPPORTED STANDARDS

- IEEE 802.1AS — gPTP (no BMCA)
- IEEE 802.1Qbv — Scheduled traffic
- IEEE 802.3 — Ethernet (GMII, MII)
- RFC 791 / 768 / 793 — IP / UDP / TCP
- RFC 826 — ARP / RFC 792 — ICMP

TRAFFIC MANAGEMENT

- Time-aware transmission scheduling (802.1Qbv)
- UDP filtering and routing
- 8 priority classes — hardware data path

OPTIONS

- DO-254 DAL-A design assurance package — on request
- Additional OS drivers (Linux, VxWorks, Windows) — on request
- IEEE 802.1Qav credit-based shaper — on request

INTERFACES

Ethernet Media	GMII (1 Gbps), MII (100 Mbp
Ethernet Ports	2 ports
Max Link Speed	1 Gbps per port
Host Interface	PCIe Gen 2 — 1 port
External Memory	None required

PERFORMANCE

Core Frequency	200 MHz
Frame Latency	50 µs (1522-byte frame)
Routing Table	Contact CetraC
QoS Levels	8 priority classes

SOFTWARE

Configuration Tools

Two tools are included to configure and deploy the IP. Both run on Linux.

- Konfyguratr — reads user parameters and generates the IP configuration file
- Loadr — loads the configuration file into the IP at runtime

Host Driver

A host driver is delivered in full C source code for the following OS:

- PikeOS — full C source code included

Drivers for other OS (Linux, VxWorks, Windows) available on request — contact CetraC.

DELIVERY PACKAGE

Core IP
IEEE 1735-2014 encrypted RTL — technology-independent

Reference Design
Example implementation on Xilinx Kintex UltraScale incl. project files & bitstream

Konfyguratr
IP configuration file generator — runs on Linux

Loadr
Configuration file loader into the IP — runs on Linux

Host Driver
Full C source code — PikeOS (other OS on request)

Documentation
Functional specification & integration guide (on request)

DO-254 DAL-A Package (option)
Not included by default — available on request

REFERENCE DESIGN

An example of implementation is provided on Xilinx Kintex UltraScale FPGA. It includes synthesis scripts, timing constraints and a ready-to-load bitstream.

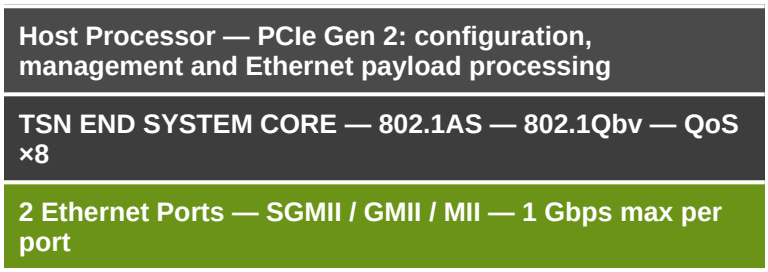
Other FPGA families and ASIC process nodes are supported — contact support@cetrac.io.

FPGA Part number	Xilinx Kintex UltraScale (XCKU040-FFVA1156-2-I)
Board Reference	Contact CetraC
SGMII	2 ports
PCIe Gen 2	Contact CetraC
LUT utilization	100k
BRAM utilization	11 Mbits
Synthesis tool	Vivado 2022.2

ARCHITECTURE OVERVIEW

Domynik TSN is a fully hardware-implemented TSN End System. Time synchronization (IEEE 802.1AS), time-aware scheduling (IEEE 802.1Qbv) and UDP/IP/ICMP/ARP filtering run in the data path at line rate with no software involvement. The PCIe Gen 2 host interface gives the host processor access to Ethernet payload and configuration registers.

The Domynik TSN IP core is delivered as IEEE 1735-2014 encrypted RTL and is not tied to any specific FPGA family or ASIC process node. Synthesis, place-and-route and timing closure are performed by the integrator on their target. A reference design on Xilinx Kintex UltraScale is provided as an integration example. Other FPGA families are supported on request — contact support@cetrac.io.



Physical interfaces depend on target platform — see Reference Design