IKARYION ARINC 664 Switch IP

14-port hardware ARINC 664/Ethernet switch IP core with full L2/L3 routing, ARINC 664 Part 7 BAG management, IP / UDP / ICMP / ARP filtering, 2-level QoS and up to 4096 routing entries.
Delivered as encrypted RTL, ITAR free technology, targeting avionics data networks.

- **14** Ethernet Ports
- **1 Gbps** Max Ethernet Link Speed
- **50 µs** Frame Latency - 1522 Bytes
- **ARINC 664p7** Compliant

KEY FEATURES

- 14-port ARINC 664/Ethernet Switch — L2/L3 routing
- 4096 routing table entries (max 512/port)
- Protocols: ARINC 664p7, IP, UDP, TCP, ICMP, ARP
- 2-level QoS traffic prioritization
- 1× AXI4 32-bit host interface
- No external memory required
- Hardware-only data path — no software latency
- Configurable BAG: 1, 2, 4, 8, 16, 32, 64, 128 ms

SUPPORTED STANDARDS

- ARINC 664 Part 7
- IEEE 802.3 — Ethernet (GMII, MII)
- RFC 791 — IP Layer 3 routing
- RFC 768 / 793 — UDP / TCP
- RFC 826 — ARP
- RFC 792 — ICMP

TRAFFIC MANAGEMENT

- Per-VL Bandwidth Allocation Gap (BAG) enforcement
- UDP filtering and routing per Virtual Link
- 2-level QoS priority classes

INTERFACES

Ethernet Media	QTBI, GMII (1 Gbps), MII (100 Mbps)
Ethernet Ports	14 ports
Max Link Speed	1 Gbps per port
Host Interface	AXI4 — 1 port, 32-bit
External Memory	None required

PERFORMANCE

Core Frequency	200 MHz
Frame Latency	50 µs (1522-byte frame)
Routing Table	4096 entries (max 512/port)
QoS Levels	2 priority classes

SOFTWARE

Configuration Tools

Two tools are included to configure and deploy the IP. Both run on Linux.

- Konfyguratr — reads user parameters and generates the IP configuration file
- Loadr — loads the configuration file into the IP at runtime

Host Driver

No host driver is included in the base delivery; the AXI4 register interface is documented for direct integration.

- Drivers (PikeOS, Linux, VxWorks, Windows…) available on request

Contact CetraC to discuss your integration needs.

DELIVERY PACKAGE

Core IP
IEEE 1735-2014 encrypted RTL — technology-independent

Reference Design
Example implementation on Altera Stratix 10 incl. project files & bitstream

Konfyguratr
IP configuration file generator — runs on Linux

Loadr
Configuration file loader into the IP — runs on Linux

Host Driver
On request (PikeOS, Linux, VxWorks, Windows)

Documentation
Functional specification & integration guide

DO-254 DAL-A Package (option)
On request — AMC 20-152A / 20-189 work also on request

REFERENCE DESIGN

An example of implementation is provided on Altera Stratix 10 FPGA. It includes the QSGMII interface, project files and a ready-to-load bitstream.

Other FPGA families and ASIC process nodes are supported — contact support@cetrac.io.

FPGA Part number	Altera Stratix 10 (1SX280HU2F50E1VGAS)
Board Reference	Contact CetraC
QSGMII	Included (QTBI ports)
AXI Data Width	32-bit
LUT utilization	143k
BRAM utilization	Contact CetraC
Synthesis tool	Quartus 2018 PRO

ARCHITECTURE OVERVIEW

IKARYION is a fully hardware-implemented ARINC 664/Ethernet L2/L3 switch. All filtering, routing and BAG-based traffic regulation (ARINC 664p7/IP/UDP/ICMP/ARP) run in the data path at line rate with no software involvement. The AXI4 host interface provides configuration and management access, and lets the host processor send and receive Ethernet payload as a switch port.

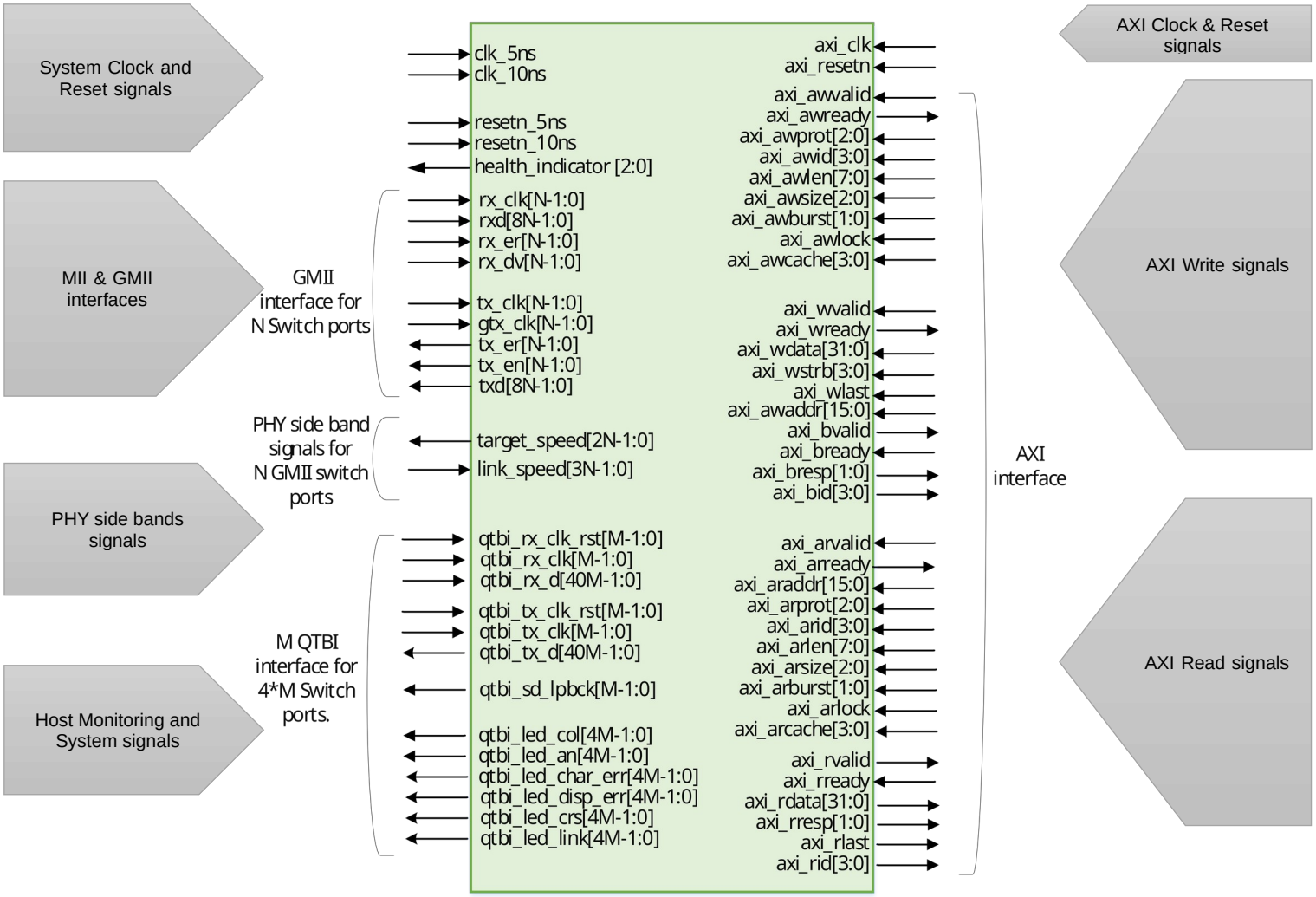
The IKARYION IP core is delivered as IEEE 1735-2014 encrypted RTL and is not tied to any specific FPGA family or ASIC process node. Synthesis, place-and-route and timing closure are performed by the integrator on their target. A reference design on Altera Stratix 10 is provided as an integration example.

Host Processor — AXI4 32-bit: configuration, management and Ethernet payload

ARINC 664 SWITCH CORE — L2/L3 — 4096 entries (max 512/port) — QoS ×2

14 Ethernet Ports — QTBI / GMII / MII — 1 Gbps max per port

Physical interfaces depend on target platform — see Reference Design



Switch ARINC 664 IKARYION IP core detailed top-level diagram