IKARYION Ethernet Switch IP

10-port hardware Ethernet switch IP core with full L2/L3 routing, IP / UDP / TCP / ICMP / ARP filtering, 2-level QoS and 512 routes per port.
Delivered as encrypted RTL, ITAR free technology and compliant with DO-254 DAL-A, AMC 20-152A and AMC 20-189.

- **10** Ethernet Ports
- **1 Gbps** Max Ethernet Link Speed
- **50 µs** Frame Latency - 1522 Bytes
- **DO-254** DAL-A Compliant

KEY FEATURES

- 10-port Ethernet Switch — L2/L3 routing
- 512 routing table entries per port
- Protocols: IP, UDP, TCP, ICMP, ARP
- 2-level QoS traffic prioritization
- 1× AXI4 64-bit host interface
- No external memory required
- Hardware-only data path — no software latency
- IEEE 1735-2014 encrypted RTL delivery

SUPPORTED STANDARDS

- IEEE 802.3 — Ethernet (GMII, MII)
- RFC 791 — IP Layer 3 routing
- RFC 768 / 793 — UDP / TCP filtering
- RFC 826 — ARP
- RFC 792 — ICMP

REGULATORY COMPLIANCE

- DO-254 DAL-A — Airborne Electronic Hardware
- AMC 20-152A — COTS IP objectives IP-1 to IP-7
- AMC 20-189 — Open Problem Reports

INTERFACES

Ethernet Media	GMII (1 Gbps), MII (100 Mbps)
Ethernet Ports	10 ports
Max Link Speed	1 Gbps per port
Host Interface	AXI4 — 1 port, 64-bit
External Memory	None required

PERFORMANCE

Core Frequency	200 MHz
Frame Latency	50 µs (1522-byte frame)
Routing Table	512 entries / port
QoS Levels	2 priority classes

SOFTWARE

Configuration Tools

Two tools are included to configure and deploy the IP. Both run on Linux.

- Konfyguratr — reads user parameters and generates the IP configuration file
- Loadr — loads the configuration file into the IP at runtime

Host Driver

A host driver is delivered in full C source code for the following OS:

- Linux — full C source code included

Drivers for other OS (PikeOS, VxWorks, Windows…) available on request — contact CetraC.

DELIVERY PACKAGE

Core IP
IEEE 1735-2014 encrypted RTL — technology-independent

Reference Design
Example implementation on XCZU11EG incl. synthesis scripts & bitstream

Konfyguratr
IP configuration file generator — runs on Linux

Loadr
Configuration file loader into the IP — runs on Linux

Host Driver
Full C source code — Linux (other OS on request)

Documentation
Functional specification & integration guide

DO-254 DAL-A Package
Full design assurance artifacts — PHAC to HAS

REFERENCE DESIGN

An example of implementation is provided on Xilinx Zynq UltraScale+ XCZU11EG MPSoC. It includes synthesis scripts, timing constraints and a ready-to-load bitstream.

Other FPGA families and ASIC process nodes are supported — contact support@cetrac.io.

FPGA Part number	Xilinx Zynq UltraScale+ (XCZU11EG-1FFVC1156 I)
Board Reference	XMC card
SGMII	8 ports
RGMII	2 ports
LUT utilization	155k (52%)
BRAM utilization	12.6 Mbits (58%)
Synthesis tool	Vivado 2022.2

ARCHITECTURE OVERVIEW

IKARYION is a fully hardware-implemented L2/L3 switch. All filtering and routing (IP/UDP/TCP/ICMP/ARP) run in the data path at line rate with no software involvement. The AXI4 host interface provides configuration and management access, and lets the host processor send and receive Ethernet payload as a switch port.

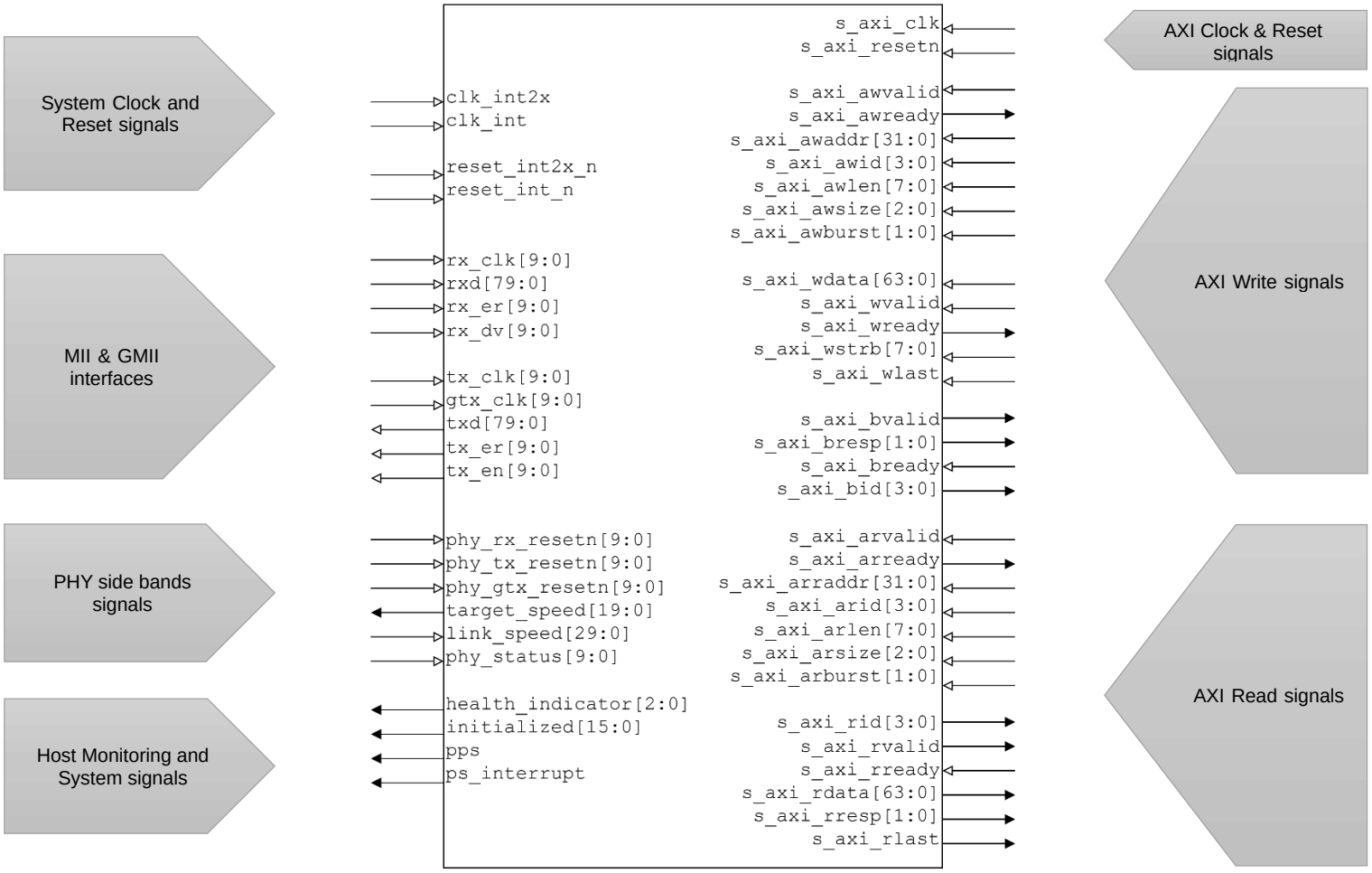
The IKARYION IP core is delivered as IEEE 1735-2014 encrypted RTL and is not tied to any specific FPGA family or ASIC process node. Synthesis, place-and-route and timing closure are performed by the integrator on their target. A reference design on Xilinx Zynq UltraScale+ is provided as an integration example.

Host Processor — AXI4 64-bit: configuration, management and Ethernet payload

SWITCH CORE — L2/L3 — 512 entries/port — QoS ×2

10 Ethernet Ports — GMII / MII — 1 Gbps max per port

Physical interfaces depend on target platform — see Reference Design



Switch Ethernet IKARYION IP core detailed top-level diagram