VEKARYON TSN Switch IP

8-port hardware Time-Sensitive Networking (TSN) Ethernet switch IP core with L2/L3 routing, IEEE 802.1AS time synchronization, IEEE 802.1Qbv time-aware scheduling, 8-level QoS and up to 4096 routing entries.
Encrypted RTL, ITAR free, for deterministic in-vehicle networks (automotive, military vehicles / NGVA).

- **8** Ethernet Ports
- **1 Gbps** Max Ethernet Link Speed
- **50 µs** Frame Latency - 1522 Bytes
- **TSN** 802.1AS / 802.1Qbv

KEY FEATURES

- 8-port TSN/Ethernet Switch — L2/L3 routing
- 4096 routing table entries (max 512/port)
- Protocols: IP, UDP, TCP, ICMP, ARP
- 8-level QoS traffic prioritization
- IEEE 802.1AS gPTP sync — no BMCA
- IEEE 802.1Qbv time-aware shaper
- Hardware-only data path — no software latency
- No external memory required

SUPPORTED STANDARDS

- IEEE 802.1AS — gPTP (no BMCA)
- IEEE 802.1Qbv — Scheduled traffic
- IEEE 802.3 — Ethernet (GMII, MII)
- RFC 791 / 768 / 793 — IP / UDP / TCP
- RFC 826 — ARP
- RFC 792 — ICMP

TRAFFIC MANAGEMENT

- Time-aware scheduling per queue (802.1Qbv)
- UDP filtering and routing
- 8 priority classes — hardware data path

INTERFACES

Ethernet Media	GMII (1 Gbps), MII (100 Mbps)
Ethernet Ports	8 ports
Max Link Speed	1 Gbps per port
Host Interface	None — configured over Ethernet ports
External Memory	None required

PERFORMANCE

Core Frequency	200 MHz
Frame Latency	50 µs (1522-byte frame)
Routing Table	4096 entries (max 512/port)
QoS Levels	8 priority classes

SOFTWARE

Configuration Tools

Two tools are included to configure and deploy the IP. Both run on Linux.

- Konfyguratr — reads user parameters and generates the IP configuration file
- Loadr — loads the configuration file into the IP over its Ethernet ports

Host Driver

No host processor interface and no driver required: the switch is configured through its Ethernet ports.

- AXI4 host interface and drivers available on request

Contact CetraC to discuss your integration needs.

DELIVERY PACKAGE

Core IP
IEEE 1735-2014 encrypted RTL — technology-independent

Reference Design
Example implementation on Altera Arria 10 incl. project files & bitstream

Konfyguratr
IP configuration file generator — runs on Linux

Loadr
Configuration file loader over Ethernet — runs on Linux

Host Driver
Not required — AXI4 + drivers on request

Documentation
Functional specification & integration guide (on request)

DO-254 DAL-A Package (option)
Not included by default — available on request

REFERENCE DESIGN

An example of implementation is provided on Altera Arria 10 FPGA. It includes the SGMII interfaces, project files and a ready-to-load bitstream.

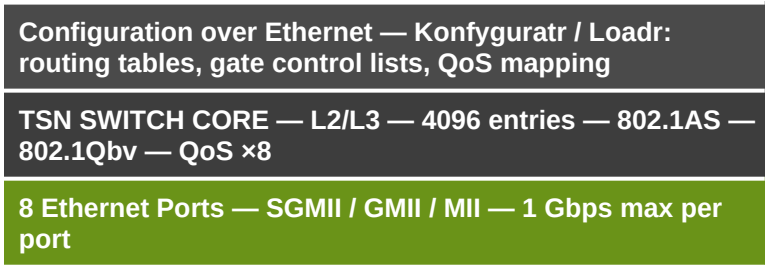
Other FPGA families and ASIC process nodes are supported — contact support@cetrac.io.

FPGA Part number	Altera Arria 10 (10AS057H2F34I1SG)
Board Reference	Contact CetraC
SGMII	8 ports
Core frequency	200 MHz
LUT utilization	150k ALM
BRAM utilization	12 Mbits
Synthesis tool	Quartus 2018 PRO

ARCHITECTURE OVERVIEW

VEKARYON is a fully hardware-implemented TSN/Ethernet L2/L3 switch. Time synchronization (IEEE 802.1AS), time-aware scheduling (IEEE 802.1Qbv), filtering and routing (IP/UDP/TCP/ICMP/ARP) run in the data path at line rate with no software involvement. Routing tables and gate control lists are generated offline by Konfyguratr and loaded by Loadr through the Ethernet ports: no host processor interface is required.

The VEKARYON IP core is delivered as IEEE 1735-2014 encrypted RTL and is not tied to any specific FPGA family or ASIC process node. Synthesis, place-and-route and timing closure are performed by the integrator on their target. A reference design on Altera Arria 10 is provided as an integration example.



Physical interfaces depend on target platform — see Reference Design